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NAVAL RESEARCH LABORATORY
ASSOCIATE COUNSEL (PATENTS)
CODE 1008.2
4555 OVERLOOK AVENUE, S.W.
WASHINGTON, DC 20375-5320

EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/715,772	DENNIS ET AL.	
	Examiner	Art Unit	
	Justin I. King	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *20 October 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. The amended claim 41 is objected to because of the following informalities: Claim 41's line 4 (Applicant's response, page 14) states "at least one peripheral units"; Applicant may have meant "at least one peripheral unit". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-41 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for each multiple thread processor to execute a plurality of instructions in one clock cycle, does not reasonably provide enablement for each processing slice to execute a plurality of instructions in one clock cycle. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-12, 14-25, 27-38, 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Butcher (U.S. Patent No. 5,421,014) and Motomura (U.S. Patent No. 5,815,727).

Referring to claim 1: Bucher discloses an apparatus comprising a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and a processing slice (Bucher claim 1's processor) coupled to the peripheral bus to execute a plurality of threads, the plurality of threads including a first thread sending the command message to the peripheral unit (Bucher claim 1).

Butcher does not explicitly disclose a functioning unit within the processing slice, but the any means for processing instruction in Butcher is the functioning unit. Furthermore, Motomura discloses a parallel processing system's processing slice (figure 1, structure 110) comprised a function unit (figure 1, structure 110) to perform a register operation (figure 5, structure 140) specified in the instructions in each of the plurality of threads, and Motomura processes the instructions from multiple thread concurrently (multiple processors in figure 1). Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention

to adapt Motomura's thread processing design to Butcher because Motomura teaches one to use multiple processors to manage the multiple threads.

Referring to claims 2-3: Claim 1's argument applies; furthermore, Bucher discloses a "read" command (column 5, line 44, figure 1, step 12) and a target peripheral (claim 1). Hence, Bucher discloses that the peripheral unit is one of an input device and an output device and the peripheral operation is one of an input operation and an output operation.

Referring to claim 4: Claim 1's argument applies; furthermore, Butcher discloses that the command messages includes at least one of a message content, a peripheral address identifying the peripheral unit, and a command code specifying the peripheral operation (figure 5).

Referring to claim 5: Claim 1's argument applies; furthermore, Butcher discloses that the peripheral information includes a response message sent from the peripheral unit to the processing slice, the response message indicating the peripheral operation is completed (abstract).

Referring to claim 6: Claims 1 and 5's arguments apply; furthermore, Butcher discloses that the response message includes at least one of a thread identifier identifying the first thread, an operation result of the peripheral operation, a data register address specifying a data register in the processing slice to store the operation result, and a length indicator indicating length of the response message (figure 5).

Referring to claim 7: Claims 1 and 5-6's arguments apply; furthermore, since Butcher discloses a SCSI bus, which is a bi-directional (claim 1).

Referring to claim 8: Butcher's disclosure is stated above. Butcher discloses that it is known to improve the performance by executing other operations while waiting for the disk

drive to locate the desired data (column 1, lines 30-36); such waiting is the claimed wait instruction. Furthermore, Motomura discloses that it is known to execute the thread in the waiting state to avoid the repeating synchronization failure or to read data in the memory used by another processor (column 1, lines 37-40); such that Motomura's waiting state is to disable the thread after sending the command message, and Motomura's instruction in the thread processing sequence is a wait instruction. Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's teaching to Butcher because Motomura teaches one to use the waiting state to avoid the repeating synchronization failure or to read data in another processor's memory.

Referring to claim 9: Butcher discloses the wait instructions for fetching the desired data (column 1,lines 30-35); thus, Butcher discloses that the waiting is not necessary while the instructions required no data fetch. Hence, Butcher discloses executing after the message sending if the message is a non-wait instruction.

Referring to claim 10: Claim 8's argument applies; furthermore, once Motomura's waiting state's pending condition met, such as the data from the memory used by another processor, Motomura's thread will continue the thread process; hence, Motomura discloses enabling the thread after receiving the response message from the peripheral unit if the thread was disabled.

Referring to claim 11: Butcher's disclosure is stated above, but Butcher does not explicitly disclose a thread control unit and instruction-processing unit fetching instructions from a program memory. The hardware component executing the Butcher's thread management logic is the thread control unit. Motomura discloses an instruction processing unit (figure 1, structures

120 and 110) to process instructions fetched from a program memory (figure 1, structure 130); and a thread control unit (figure 16's thread execution control system) coupled to the instruction processing unit to manage initiating and termination of at least one of the plurality of threads. Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's thread processing design to Butcher because Motomura teaches one to use the thread control unit to manage the waiting state to avoid the repeating synchronization failure or to read data in another processor's memory.

Referring to claim 12: Claim 11's argument applies; furthermore, Butcher discloses saving the final information of the completed command in data structure (figure 3, step 52); Butcher's data structure is the register file having a plurality of data registers for storing the thread result, and Butcher's data structure's interface for connecting the data structure to a bus is the data memory switch. Butcher does not explicitly disclose a memory access unit and the functioning unit. Motomura discloses a memory access unit (figure 16, structure 620) coupled to the instruction processing unit to provide access to one of a plurality of data memories (figure 16, structure 1420) via a data memory switch (figure 16, structure 1420's interface to structure 620), the memory access unit having a plurality of data base registers (figure 16, structure 1610), each of the data base registers corresponding to each of the threads; and a functional unit (figure 1, structures 110) coupled to the instruction processing unit to perform an operation specified in one of the instructions; and a register file (figure 16, structure 1610) having a plurality of data registers (figure 15, structures 541 and 1341), each of the data registers corresponding to each of the threads. Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's thread processing design to Butcher because

Motomura teaches one to use the thread control unit to manage the waiting state to avoid the repeating synchronization failure or to read data in another processor's memory.

Referring to claim 14: Claim 1's argument applies; Bucher discloses a method comprising a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and a processing slice coupled to the peripheral bus to execute a plurality of threads, the plurality of threads including a first thread sending the command message to the peripheral unit (Bucher's claim 1).

Referring to claims 15-16: Claim 14's argument applies; furthermore, Bucher discloses a "read" command (column 5, line 44, figure 1, step 12) and a target peripheral (claim 1). Hence, Bucher discloses that the peripheral unit is one of an input device and an output device and the peripheral operation is one of an input operation and an output operation; therefore, claims 15-16 are anticipated by Butcher.

Referring to claim 17: Claim 14's argument applies; furthermore, Butcher discloses that the command messages includes at least one of a message content, a peripheral address identifying the peripheral unit, and a command code specifying the peripheral operation (figure 5).

Referring to claim 18: Claim 14's argument applies; furthermore, Butcher discloses that the peripheral information includes a response message sent from the peripheral unit to the processing slice, the response message indicating the peripheral operation is completed (abstract).

Referring to claim 19: Claims 14 and 18's arguments apply; furthermore, Butcher discloses that the response message includes at least one of a thread identifier identifying the first

thread, an operation result of the peripheral operation, a data register address specifying a data register in the processing slice to store the operation result, and a length indicator indicating length of the response message (figure 5).

Referring to claim 20: Claims 14 and 18-19's arguments apply; furthermore, since Butcher discloses a SCSI bus, which is a bi-directional (claim 1).

Referring to claim 21: Claim 21 is rejected as the claim 8's argument above.

Referring to claim 22: Butcher discloses a command pending status (figure 1, step 20) and a loop back to issue more command (figure 1, step 18). Butcher's step 20 and the loop back is the non-wait instruction. Hence, Butcher discloses that the first thread continues to execute after sending the command message if the command message is a non-wait instruction

Referring to claim 23: Claim 23 is rejected over the claim 10's argument above.

Referring to claim 24: Claim 24 is rejected over the claim 11's argument above.

Referring to claim 25: Claim 25 is rejected over the claim 12's argument above.

Referring to claim 27: Claim 27 is rejected over the claim 1's argument above. Furthermore, Bucher discloses an apparatus comprising a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and a processing slice coupled to the peripheral bus to execute a plurality of threads, the plurality of threads including a first thread sending the command message to the peripheral unit (claim 1). But Butcher does not explicitly disclose a plurality of banks of data memory; a data memory switch coupled to the banks to data memory; a program memory to store a program. Motomura discloses a plurality of banks of data memory (figure 16, structure 1420), a data memory switch (figure 16, structure 1420's interface to other component) coupled to the

banks to data memory; a program memory to store a program (figure 1, structure 130). Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's thread processing design to Butcher because Motomura teaches one to use the thread control unit to manage the waiting state to avoid the repeating synchronization failure or to read data in another processor's memory.

Referring to claims 28-29: Claim 27's argument applies; furthermore, Bucher discloses a "read" command (column 5, line 44, figure 1, step 12) and a target peripheral (claim 1). Hence, Bucher discloses that the peripheral unit is one of an input device and an output device and the peripheral operation is one of an input operation and an output operation.

Referring to claim 30: Claim 27's argument applies; furthermore, Butcher discloses that the command messages includes at least one of a message content, a peripheral address identifying the peripheral unit, and a command code specifying the peripheral operation (figure 5).

Referring to claim 31: Claim 27's argument applies; furthermore, Butcher discloses that the peripheral information includes a response message sent from the peripheral unit to the processing slice, the response message indicating the peripheral operation is completed (abstract).

Referring to claim 32: Claims 27 and 31's arguments apply; furthermore, Butcher discloses that the response message includes at least one of a thread identifier identifying the first thread, an operation result of the peripheral operation, a data register address specifying a data register in the processing slice to store the operation result, and a length indicator indicating length of the response message (figure 5).

Referring to claim 33: Claims 27 and 31-32's arguments apply; furthermore, since Butcher discloses a SCSI bus, which is a bi-directional (claim 1).

Referring to claim 34: Claim 27's argument applies; furthermore, claim 34 is rejected over the claim 8's argument as stated above.

Referring to claim 35: Claim 27's argument applies; furthermore, Butcher discloses a command pending status (figure 1, step 20) and a loop back to issue more command (figure 1, step 18). Butcher's step 20 and the loop back is the non-wait instruction. Hence, Butcher discloses that the first thread continues to execute after sending the command message if the command message is a non-wait instruction

Referring to claim 36: Claims 27 and 34's arguments apply; furthermore, claim 36 is rejected over the claim 10's argument stated above.

Referring to claim 37: Claim 27's argument applies; furthermore, claim 37 is rejected over the claim 11's argument as stated above.

Referring to claim 38: Claims 27 and 37's arguments apply; furthermore, claim 38 is rejected over the claim 12's argument stated above.

Referring to claim 40: Bucher discloses an apparatus comprising a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and a processing slice coupled to the peripheral bus to execute a plurality of threads, the plurality of threads including a first thread sending the command message to the peripheral unit (Butch claim 1). Butcher discloses a SCSI controller (Butch claim 1), and the SCSI controller's processing chip is the multi-thread processor, and the SCSI devices are the peripheral units. Butcher does not explicitly disclose that the system has a plurality of the multi-

thread slices. Motomura discloses a plurality of multi-thread processors (figure 1, structures 110), which is the claimed multiple thread slices. In addition, court has held that the duplication of essential component only involves ordinary skill in the art (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8).

Motomura discloses a parallel processing system with multiple processing slices (figure 1) and each processing slice (figure 1, structure 110) comprised a function unit (figure 1, structure 110) to perform a register operation (figure 5, structure 140) specified in the instructions in each of the plurality of threads, and Motomura processes the instructions from multiple thread concurrently (multiple processors in figure 1). Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's thread processing design to Butcher because Motomura teaches one to use multiple processors to manage the multiple threads.

Referring to claim 41: Claim 41 is rejected over the claims 1 and 40's arguments above. Furthermore, Bucher discloses an apparatus comprising a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and a processing slice coupled to the peripheral bus to execute a plurality of threads, the plurality of threads including a first thread sending the command message to the peripheral unit (claim 1). Butcher does not explicitly disclose program base registers and database registers. Motomura discloses program base registers (figure 15, structure 140) and database registers (figure 16, structure 1610). Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's thread processing

design to Butcher because Motomura teaches one to use the thread control unit to manage the waiting state to avoid the repeating synchronization failure or to read data in another processor's memory.

6. Claims 13, 26, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Butcher, Motomura, and Hiraoka et al. (U.S. Patent No. 5,418,917).

Referring to claims 13, 26, and 39: Butcher and Motomura's disclosures are stated above; furthermore, Butcher does not explicitly disclose an instruction fetch unit, buffer, decoder, dispatcher, and execution concurrently in a clock cycle. Motomura discloses an instruction fetch unit (figure 5, structure 150) to fetch the instructions from the program memory using a plurality of program counters (figure 15, structure 140), each program counter corresponding to each of the threads; an instruction decoder (figure 5, structure 542) and dispatcher (figure 5, structure 150) to decode the instructions and dispatch the decoded instructions to one of the memory access unit, the functional unit, and the peripheral unit. Since Motomura discloses a plurality of processors (figure 1, structures 110), Motomura discloses that multiple instructions are executed concurrently in a clock cycle. Motomura does not disclose the instruction buffer. Hiraoka discloses that the instruction buffer is a well-known industrial practice (figure 1). Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Motomura's thread processing design and Hiraoka's instruction buffer to Butcher because they teach one to use the thread control unit to manage the waiting state to avoid the repeating synchronization failure or to read data in another processor's memory and to enhance instruction processing with an instruction buffer.

Response to Arguments

7. In response to Applicant's argument that the processor slice is able to process several threads simultaneously (Remark, page 17, paragraphs 1, 4): In view the Specification page 8, paragraphs 2 and 3, each processor includes four processing slice, which enables the processor to execute multiple instructions from multiple threads within one clock cycle. The Specification page 8 line 23 discloses that each processing slice uses the interleave technique to process instructions. The interleave technique makes each processing slice available for every thread's instructions, but it does not enables each processing slice executing multiple instructions simultaneously. The multiple processing slices enable the processor to execute the multiple instructions simultaneously. Hence, the Specification does not support the alleged processing slice's ability to execute multiple instructions simultaneously.

8. In response to Applicant's argument that Butcher's wait and non-wait instruction (Remark, page 17, last paragraph): Butcher discloses the wait instructions for fetching the desired data (column 1,lines 30-35); thus, Butcher discloses that the waiting is not necessary while the instructions required no data fetch. Hence, Butcher discloses executing after the message sending if the message is a non-wait instruction.

9. In response to Applicant's argument that the prior arts do not disclose the processor slice, and the each Motomura's executing thread has its own functional unit which does not perform operations from any other thread (Remark, page 18, paragraph 4): The Motomura discloses a parallel processing system. Each Motomura's processor is equivalent to Applicant's processing slice, and Motomura's parallel processing system is equivalent to Applicant's processor. Motomura's parallel processing system executes multiple instructions simultaneously.

Motomura discloses that each processing slice does process operations from other threads while the first thread is in the waiting state (column 2, lines 56-58).

10. In response to Applicant's argument that Motomura discloses a plurality of single-thread processors (Remark, page 18, paragraph 5): As discussed above, each Motomura's processor is equivalent to the claimed processing slice, and Motomura explicitly discloses that each processor executes the second thread while the first thread is in the waiting state (column 2, lines 56-58). Hence, Motomura's processors are multiple-threaded.

11. In response to Applicant's argument that Hiraoka does not disclose the claimed processor slice (Remark, page 18, last paragraph): Hiraoka is applied to support the practice of the instruction buffers.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Mark Reinhart can be reached at (703) 308-3110.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
December 22, 2003

XUAN M. THAI
PRIMARY EXAMINER